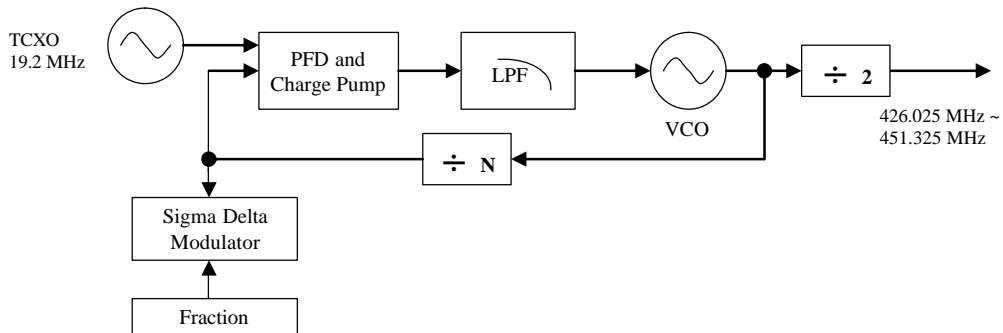


Phase Lock Loop for UHF Radio

Fact Sheet

Process	0.25 μm CMOS
What Challenge	Low Phase Noise PLL Low phase noise (< -90 dBc/Hz @ 12.5 KHz offset)

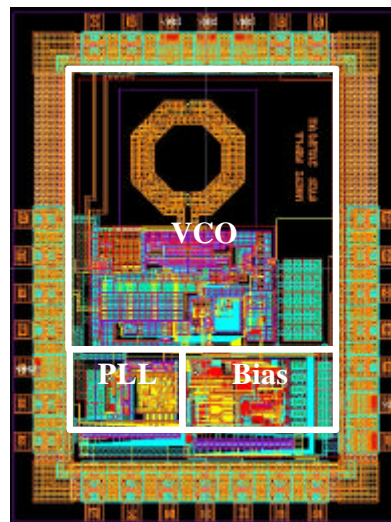
Description



The block diagram of the Fractional N PLL implementation (with on chip VCO) is as shown above.

By adopting a Fractional N architecture by means of a 3-stage 16 bit MASH sigma delta modulator as shown above, the output frequency can be derived directly from the 19.2 MHz reference. A Dual Modulus divider is designed consisting of a Divide 4/5 TSPC Prescaler, a 4 bit Programmable and a 2 bit Swallow Counter.

As the PFD input frequency is now 19.2 MHz, a maximum PLL closed loop bandwidth of about 1.92 MHz is theoretically achievable. However, as the effect of the sigma delta modulator will push the quantisation noise into higher offset frequencies, the loop bandwidth is limited to about 100 KHz range. The chip layout is as shown below.



PLL Subcircuit Layout